IN THE ABSTRACT:

Please replace the Abstract of the Disclosure originally filed with the above-identified patent application with the following new Abstract of the Disclosure:

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a high-K gate dielectric layer includes a p-type well that is formed in an upper layer of a silicon substrate. Arsenic ions are implanted into an extreme surface layer of the p-type well and a heat treatment is performed to form a p-type low-concentration layer. A HfAlOx film and a polycrystalline silicon layer are laminated on the substrate. A gate electrode is formed by patterning the polycrystalline silicon layer. After a n-type extension region is formed by implanting arsenic ions by using the gate electrode as a mask, sidewall spacers are formed on sides of the gate electrode. Arsenic ions are implanted by using the sidewall spacers and the gate electrode as masks, whereby n-type source/drain regions are formed.